REMARKS

This is in response to the Office Action dated May 21, 2004. Claims 1, 3, 5, 7-9, 11-19, 29, 31-46 and 49-56 are pending.

It is respectfully requested that the Examiner confirm that the IDS filed August 10, 2001 has been considered, by providing the undersigned with an initialed copy of the PTO-1449 corresponding to the same.

Example Non-Limiting Embodiments (for ease of understanding)

For purposes of example only, and without limitation, certain example embodiments of this invention relate to a semiconductor memory device. Referring to the embodiment of Figs. 1 and 73 for example, a semiconductor memory device includes a plurality of memory cells (e.g., EEPROMs) stacked on semiconductor substrate 100. As shown in Figs. 1 and 73, an example memory cell includes an island-shaped semiconductor layer(s) 110 which extends vertically relative to the semiconductor substrate 100, a charge storage layer(s) (e.g., floating gate 510), and a control gate(s) 520. It can be seen from Figs. 1 and 73 that the charge storage layer 510 (or 513) and the control gate 520 (or 523) laterally surround a vertically extending sidewall of island-like semiconductor layer 110 as viewed from above. Insulating layer 610 (or 613), including one or more insulators, is located between the control gate 520 (or 523) and the charge storage layer 510 (or 513). In Fig. 78, a pair of memory cells are located in the central portion of the stack, while first and second selection transistors using gate electrodes 500 are located at the top and bottom of the stack, respectively.

According to certain example non-limiting embodiments of this invention, the active region of at least one of the memory cells in the stack is electrically insulated form the semiconductor substrate 100 (e.g., pg. 47, lines 4-28; pg. 48, lines 4-18; pg. 92, lines 10-14; pg. 95, lines 11-27). In certain example embodiments, the active region of a memory cell may be electrically insulated from the semiconductor substrate by *both* (a) a diffusion layer formed in the semiconductor substrate or the island-like semiconductor layer, and (b) a ***depletion layer*** formed at a junction between the diffusion layer and the semiconductor substrate or the island-like semiconductor layer. In the Fig. 97-98 embodiment, the island-like semiconductor layer 110 and the semiconductor substrate 100 become in an electrically floating state due to a *depletion layer* formed on the substrate or semiconductor layer of a PN junction formed between diffusion layer 710 and substrate 100 or semiconductor layer 110 by a difference between a potential given to diffusion layer 710 and a potential given to substrate 100 at times of reading and/or erasing (e.g., pg. 95, lines 11-27). Such structure is advantageous in that a back-bias effect in a semiconductor memory having charge storing layer(s) and control gate(s) can be reduced, and capacity between floating gates and control gates may be increased without significantly increasing the occupied area and variations in characteristics of memory cells may be suppressed (e.g., pg. 16, lines 19-24).

In certain example embodiments of this invention, first and second selection transistors are located on opposite vertical sides of a plurality of memory cells in a vertical direction so as to sandwich the plurality of memory cells therebetween. For

example, Fig. 73 illustrates selection gates 500 for first and second transistors which sandwich a pair of memory cells therebetween in a vertical direction.

Allowed Claims

Applicant notes with appreciation the Examiner's allowance of claims 19, 37-39 and 55. It is assumed that claim 56 has also been allowed since it depends on allowed claim 55.

Claim 1

Claim 1 stands rejected under 35 U.S.C. Section 102(b) as being allegedly anticipated by Burns (US 5,990,509). This Section 102(b) rejection is respectfully traversed for at least the following reasons.

Claim 1 requires that the active region of said memory cell is electrically insulated from the semiconductor substrate by: (a) a second conductivity type impurity diffusion layer formed in the semiconductor substrate or in the island-like semiconductor layer and (b) means for forming a depletion layer formed at a junction between the second conductivity type impurity diffusion layer and the semiconductor substrate or the island-like semiconductor layer." The cited art fails to disclose or suggest this aspect of claim 1.

Burns clearly fails to disclose or suggest the insulating "depletion layer" recited in claim 1 for electrically insulating the active region of the memory cell from the semiconductor substrate. Burns discloses nothing akin to this aspect of claim 1, and is entirely unrelated thereto.

In the Office Action dated May 21, 2004, on page 3, the Examiner contends that the formation of the depletion layer is "merely the intended use" and can be ignored. This allegation is respectfully traversed. Claim 1 calls for (b) *means for forming a depletion layer formed at a junction between the second conductivity type impurity diffusion layer and the semiconductor substrate or the island-like semiconductor layer.*" This requirement of claim 1 is in means-plus-function form pursuant to 35 U.S.C. Section 112, paragraph 6, and cannot be ignored by the Examiner as an "intended use." The statute permits a claim to be written in such a manner, and required that the Examiner consider the same as a positively recited claim limitation. The reference fails to disclose or suggest this requirement of claim 1.

In the Office Action dated May 21, 2004, on page 3, the Examiner contended that Burns in Fig. 10 discloses a pn junction between diffusion layer 215 and substrate 235, and that this "implies that there exists a pn junction therein." *However*, in Fig. 10 of Burns the substrate 235 and the pillar 230 are electrically insulated not by the pn junction, but rather only by the diffusion layer 215 itself. Thus, it will be appreciated that *Burns fails to disclose or suggest electrically insulating the pillar 230 from the substrate 235 by extending a depletion layer as recited in claim 1.* Burns is entirely unrelated to the invention of claim 1 in this regard.

The electrical insulating by the depletion layer may result in significant advantages in the art. For example, the use of the claimed depletion layer to insulate may result in improved thermal performance. Moreover, depending on bias conditions, it is

possible to make use of an electrical connection of the substrate and pillar-shaped semiconductor layer so as to broaden the application range of the semiconductor device(s). These example advantages are not achievable in the cited art.

Other Claims

Burns also fails to disclose or suggest the claimed means for forming the depletion layer . . . as recited in claims 5, 36, 46. As explained above, Burns is entirely unrelated to this aspect of these claims.

Conclusion

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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